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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,088	02/05/2004	Mitsuru Okigawa	81784.0301	3288

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/773,088	OKIGAWA, MITSURU
	Examiner	Art Unit
	Luan Thai	2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/5/04&3/8/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The Information disclosure Statements filed on 2/5/04 and 3/08/05 have been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (6,239,366).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 9, 12, and 14, Hashimoto (see specifically figures 7-11 and 13) discloses a semiconductor integrated device, provided with a semiconductor chip (40) on which a semiconductor integrated circuit is formed and a support substrate (80/82) laminated on at least one surface of the semiconductor chip, wherein resin (46) that is a mixture of micro particles (Col. 18, lines 50+) is filled between the semiconductor chip (40) and the support substrate

(80/82), and a distance between the semiconductor chip and the support substrate is larger than the maximum particle diameter of the micro particles (see figures 7-11 and 13) at least at an effective element region within the semiconductor chip where the semiconductor integrated circuit is formed. Hashimoto further discloses another resin (88) not containing micro particles (see figure 11).

5. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamaki et al. (6,157,080).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-4, Tamaki et al. (see specifically figures 20A-20B) discloses a semiconductor integrated device, provided with a semiconductor chip (1) on which a semiconductor integrated circuit is formed and a support substrate (19) laminated on at least one surface of the semiconductor chip, wherein resin (9) that is a mixture of micro particles (25) is filled between the semiconductor chip (1) and the support substrate (19), and a distance between the semiconductor chip and the support substrate is larger than the maximum particle diameter of the micro particles (see figure 20B) at least at an effective element region within the semiconductor chip where the semiconductor integrated circuit is formed. Tamaki et al. further disclose another resin (15) not containing micro particles.

6. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaminaga et al. (6,321,734).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-2, Kaminaga et al. (see specifically figure 1) discloses a semiconductor integrated device, provided with a semiconductor chip (1) on which a semiconductor integrated circuit is formed and a support substrate (3) laminated on at least one surface of the semiconductor chip (1), wherein resin (4) that is a mixture of micro particles (11) is filled between the semiconductor chip (1) and the support substrate (3), and a distance between the semiconductor chip and the support substrate is larger than the maximum particle diameter of the micro particles (see Abstract) at least at an effective element region within the semiconductor chip where the semiconductor integrated circuit is formed.

7. Claims 1-6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hikita et al. (6,133,637).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-6 and 8, Hikita et al. (see specifically figures 22-26 and 50-54) discloses a semiconductor integrated device, provided with a semiconductor chip (14) on which a semiconductor integrated circuit is formed and a support substrate (16) laminated on at least one surface of the semiconductor chip (14), wherein resin (24) that is a mixture of micro particles (80) is filled between the semiconductor chip (14) and the support substrate (16), and a distance between the semiconductor chip and the support substrate is larger than the maximum particle diameter of the micro particles (80) at least at an effective element region within the semiconductor chip where the semiconductor integrated circuit is formed, and another resin (22) not containing micro particles (see figure 11). Hikita et al. further discloses a method of manufacturing such semiconductor integrated device (see specifically figures 22-26 and 50-54),

comprising: a first step of coating resin (24) mixed with micro particles (80) on at least one surface of the semiconductor substrate (14) on which the semiconductor integrated circuit is formed, and laminating the support substrate (16) on the semiconductor substrate (14) to hold the resin between the two substrates; and a second step of pushing the support substrate (16) against the semiconductor substrate (14), wherein in the second step, the support substrate is pushed against the semiconductor substrate while keeping a distance between the semiconductor substrate and the support substrate larger than the maximum particle diameter of the micro particles (80). The method of manufacturing the semiconductor device above further comprising a step of hardening the resin (24) by subjecting heat treatment process after the second step (Col. 10, lines 27+), and wherein in the second step the distance between the semiconductor substrate and the support substrate is kept larger than the sum of a contraction amount by which the film thickness of the resin contracts during the hardening step and the maximum particle diameter of the micro particles (see figures 23 and 25-26). Hikita et al. further disclose the step of coating a second resin layer (22) not containing micro particles on the first resin layer hardened (24).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (6,133,637) in view of Fujimoto et al. (5,930,599).

Regarding claims 7 and 9, Hikita et al. disclose the claimed invention as detailed above except for a step of etching the semiconductor substrate.

Fujimoto et al. while related to a similar semiconductor structure teach (see specifically figures 1-6) a method of manufacturing a semiconductor device including a step of etching the semiconductor substrate (20) to reduce the thickness of the semiconductor substrate and thus, the device is reduced (Col. 8, lines 63-67 and Col. 9, lines 1-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Fujimoto et al.'s teachings of etching step to Hikita et al.'s method in order to reduce semiconductor device, and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2891
August 20, 2005